REMARKS

Claims 1-4, 6-8, 11-13, 15-21 and 23 are pending.

Claims 1-7 and 16 have been amended herein and, as amended, are fully supported in the detailed description. The specification has been amended herein. No new matter has been added to the specification as a result of these amendments.

35 U.S.C. §132

Applicant's amendment filed 29 January 2003 has been objected to under 35 U.S.C. §132 as introducing new matter. Examiner states that the added material which is not supported by the original disclosure is the limitation that the "voltage pull-up device is implemented as a transistor with less than 1.0 V_{BE}."

Examiner states that "there is no ' pull-up device' found to be disclosed that is a 'transistor'," and that the "only element found to be disclosed that is a 'pull-up device' that meets the claim limitations is element 214, 314." Examiner further states that "there is no disclosure of element 214 or 314 being a transistor" and that the Examiner "agrees that element 309 is a pull-up element that can be 'implemented as a transistor with less than 1.0 Vbe.'"

Applicant respectfully directs Examiner's attention to Applicant's original disclosure, page 11, lines 5 & 6, which states, "The current source shown at 214 is implemented in this illustration as a MOSFET current source." The term MOSFET is a term of art widely understood to stand for "Metal oxide/silicon field effect transistor." (Emphasis added.) Applicant maintains that, by disclosing element 214 as a MOSFET, element 214 was fully and originally disclosed as a transistor.

Further, Applicant respectfully directs Examiner's attention to Applicant's original disclosure, page 14 lines 11 to 14, where it is stated that "The combination of device 320 and transistor 309 acts to pull the VBE of transistor 310 towards VCC which means that the buffering that is done by transistor 310 can be accomplished at a lower VCC." (Emphasis added.) Also, to page 13 line 21 to page 14, line 2, where it is stated that "device 320 is necessary to pull the voltage back up and prevent saturation of transistors 201 and 202. Device 320 can be

implemented, in various embodiments, as a resistor or as a transistor with less than 1 VBE." Element 320 is, therefore disclosed as a pull-up device that can be implemented as a transistor with less than 1 VBE.

Element 214, 314 is, therefore, fully disclosed as a transistor by the above referenced portion of Applicant's original disclosure. Element is disclosed as a pull-up device, which can be implemented as a transistor, with less than one 1 VBE. Thus, no new matter was entered as a result of the amendment filed 29 January 2003. Examiner's rejection under 35 U.S.C. §132 is therefore, respectfully traversed.

However, in order to more clearly delineate the disclosure, Applicant respectfully requests the entry of the amended paragraphs requested above. No new matter is entered as a result of these amendments.

Claim Objections

Claim 1 is objected to because the phrase "less than 1.0 VBE" is confusing. Claim 7 is objected to for similar reasons as Claim 1. Claims 2-4, 6, 8 and 11-15 are objected to for the reasons discussed with Claims 1 and 7, from which they depend. Applicant ahas amended the Claims objected to in accordance with Examiner's recommendation.

35 U.S.C. §103

Claims 1-4, 6-8, 11-13, 15-21 and 23 have been rejected under 35 U.S.C. §103(a) as being unpatentable, as obvious, over U.S. Patent 5,621,308 to Kadanka et al in view of newly cited U.S. Patent 5,666,046 to Mietus.

Regarding Claims 1, 7 and 16, Kadanka et al. disclose a circuit comprising: "a band-gap reference circuit"; "a buffer circuit;" and "a voltage pull-up device" wherein the "voltage pull-up device" has a "transistor". Kadanka et al. does not expressly disclose that the transistor has a "less than 1.0 Vbe" but it is taught by Mietus to use a voltage of 0.7 volts for the expected advantage of using a lower supply voltage (Col. 1, lines 56-67).

The present application, however, claims a "a low impedance band-gap reference circuit," "a buffer circuit," and "a voltage pull-up device" wherein the voltage pull-up device is electronically coupled between said band-gap reference circuit and said buffer circuit. By disposing the pull-up device between the reference circuit and the buffer, as claimed in Claim 1 and supported in specification (see Figure 3), Applicant avers that the advantage of low impedance found in the claimed disposition is a result unexpected by Kadanka and Mietus, and is not taught, either alone or in combination. Examiner's rejection of Claims 1, 7, and 16 is, therefore, respectfully traversed.

Regarding Claims 2–4, 6, 8, 11–13, 15, 17-21 and 23, these are dependent claims, dependent from independent claims which are, as amended, in condition for allowance. As such, they are allowable limitations on those claims and the rejections of record are respectfully traversed.

CONCLUSION

In light of the foregoing amendments and remarks, Applicant respectfully submits that the remaining claims are in condition for allowance. Applicant respectfully requests allowance of the pending Claims.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Date: SEPT 25, 2003

Respectfully submitted,

Michael R. Hardaway
Reg. No. 52,992
WAGNER, MURABITO & HAO LLP
Two North Market Street, 3rd Floor
San Jose, California 95113
(408) 938-9060